referred to as NMOS) in which a gate electrode formed on a P-type semiconductor substrate is comprised of N+ type polycrystalline silicon and a P-channel MOS transistor 212 (hereinafter referred to as PMOS) in which a gate electrode formed in an N-well region is also comprised of N+type polycrystalline silicon, and a resistor 215 used in a voltage dividing circuit for dividing a voltage which is formed on a field insulating film or a CR circuit for setting a time constant. The resistor is formed of a polycrystalline silicon that is the same layer as a gate electrode of CMOS with N-type conductivity and has the same conductivity type in terms of simplicity and ease of a method of manufacturing thereof.--

B' cont

Please replace the paragraph beginning at page 2, line 20, with the following rewritten paragraph:

B2

--In the buried channel E-type PMOS, in the case where the threshold voltage is set to, for example, -0.5 V or more for low voltage operation, a sub-threshold characteristic, which is one index of low voltage operation of a MOS transistor, extremely deteriorates, and thus, a leak current at the off time the PMOS increases. As a result, consumption current at the time of waiting of the semiconductor device remarkably increases. Thus, there is a problem in that it is difficult to apply the semiconductor

device to portable apparatuses typified by a portable telephone and a portable terminal which re greatly demanded in recent years and the market for which is predicted to further develop in the future.--

Please replace the paragraph beginning at page 95, line 5, with the following rewritten paragraph:

--P+polycrystalline silicon that is a source and a gate of the D-type NMOS 126 is short-circuited by a wiring metal though not shown in the figure, and further, the drain is connected with a high voltage supply terminal 123 showing the D-type NMOS 126.--

IN THE CLAIMS:

Kindly amend claims 1, 2, 4, 11, 15, 16, 43 and 54 as follows:

1. (Amended) A complementary MOS semiconductor device for a voltage regulator, comprising: a semiconductor substrate; an N-channel MOS transistor formed in the semiconductor substrate and used in a reference voltage generating circuit of the voltage regulator; a P-channel MOS transistor formed in the semiconductor substrate and used as an output element of the voltage regulator; and a resistor formed in the semiconductor substrate; wherein a conductivity